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(54) **An output buffer with constant switching current**

Ausgangspuffer mit Konstantschaltstrom

Tampon de sortie à courant de commutation constant

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(56) References cited:
EP-A- 0 331 341
EP-A- 0 597 590
EP-A- 1 032 132
WO-A-98/37632
US-A- 5 061 864
US-A- 5 338 978
US-A- 5 367 210
US-A- 6 040 729

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Description

[0001] The present invention relates to integrated circuits and, more particularly, to an output buffer for digital signals as defined in the preamble of Claim 1.

[0002] Document US-A-5 367 210 and EP-A-0 331 341 disclose an output buffer as defined in the preamble of claim 1.

[0003] As is known, in an integrated circuit, an output buffer for digital signals is an interface circuit which serves for driving a load which, in most cases, is outside the integrated circuit. Normally, the circuit is dimensioned on the basis of direct-current operating specifications, that is, on the basis of the maximum value of the supply voltage and on the maximum value of the current to be supplied to a predetermined resistive load. As a result of this dimensioning, the switching speed is often much greater than required and this may give rise to serious disadvantages. In particular, as the number of functions which can be integrated in a single chip of semiconductor material increases, the number of outputs of the integrated device increases. The outputs are often grouped in "buses" and have to be switched simultaneously by the respective output buffers. In these cases, very high pulsed currents pass through the impedances and the parasitic resistances associated with the electrical connections between the integrated circuit and the external terminals during switching. These current transients require the external supply to deliver, for very short periods, currents much greater than those required on average for the operation of the device, and therefore necessitate the use of over-dimensioned supply means. This problem is experienced in particular when the integrated device forms part of portable apparatus, that is, of apparatus having limited electrical energy resources. Moreover, the current transients may give rise to spurious internal switching, and hence to losses or alterations of the data associated with the digital signal. In mixed integrated circuits, that is, those containing both digital portions and analog portions, the current transients may prejudice the performance of the analog circuits.

[0004] To prevent or at least attenuate the problems explained above, devices must be designed with supply-connection tracks of sufficiently large cross-section. A solution cf this type is completely unsatisfactory since it leads to a great wastage of area and does not solve the problem of excessive demands on the supply.

[0005] A known output buffer designed to address the problems explained above is shown in Figure 1. In this example, the buffer is constituted by four pairs of complementary MOS transistors connected so as to operate in phase opposition, in pairs (M1n-M4n; M1p-M4p), but it could be constituted by a much larger number of such pairs. The pairs of transistors are connected between two supply terminals, indicated by the earth symbol and +VDD, and have, as a common terminal, the drain electrodes of the transistors which are connected to an output terminal OUT. The gate electrodes of the first pair M1p, M1n are connected together to the input terminal IN of the buffer and the gate electrodes of the subsequent pairs are connected together to the gate electrodes of the respective preceding pairs by means of delay circuits which, in this example, have equal delay times Δt. The transistors are of a size such that each pair can supply one quarter of the output current to the load, not shown. As a result of the delays, a transition in the level of a signal applied to the input IN gives rise to a much slower transition in the output signal than in the input signal, reducing any current peaks. However, this circuit operates satisfactorily only if it is constituted by a large number of pairs of transistors. This involves the wastage of a large area of the integrated circuit so that this solution is not in practice very much favoured by designers.

[0006] Another known buffer is shown schematically in Figure 2. It is formed by a single pair of complementary MOS transistors Mp and Mn controlled by respective driver stages DRp and DRn. The stages DRp and DRn operate in a manner such as to switch the respective transistors off rapidly and to switch them on slowly by the generation of a constant-current front long enough to cause the output OUT to switch gradually. However, this known buffer is rather complex and, in the same manner as the other known buffer described briefly above, supplies a current which varies in dependence on the load.

[0007] An object of the present invention is to propose an output buffer for digital signals in which the switching current, that is, the current delivered or absorbed during the transitions of the digital signal, is independent of the load.

[0008] Another object is to propose an output buffer for digital signals which is simple and reliable and occupies a small area.

[0009] These objects are achieved by the provision of the buffer defined and characterized in general in Claim 1.

[0010] The invention will be understood further from the following detailed description of two embodiments thereof, given by way of non-limiting example, with reference to the appended drawings, in which:

figures 1 and 2 show the circuits of two known buffers,
figure 3 shows the circuit cf a buffer according to a first embodiment of the invention,
figure 4 shows some wave-forms which illustrate the operation of the circuit of Figure 3,
figure 5 shows a second embodiment of the invention, and
figure 6 shows the circuit of a possible practical implementation of the embodiment of Figure 5.

[0011] The circuit shown in Figure 3 comprises an output stage 10 with complementary MOSFET transistors,

more precisely, a p-channel transistor MPOUT and an n-channel transistor MNOUT, connected so as to operate in phase opposition between a first supply terminal +VDD and a second supply terminal, indicated by the earth symbol. The node common to the two transistors, that is, the connection node between their two drain electrodes, is the output terminal OUT of the buffer and is connected, by means of a respective pin of the integrated circuit, to an external load 13, typically a substantially capacitive load.

[0012] The circuit comprises two stages 14 and 15 for driving the transistors of the output stage 10. The driver stage 14 is constituted by two circuit branches: a first circuit branch comprises an n-channel MOS transistor MN4 and a p-channel MOS transistor MP1. The transistor MN4 which, as will be explained below, has the function of generating current, has its source electrode connected to earth, its drain electrode connected to the gate electrode of the output transistor MPOUT, and its gate electrode connected to the input terminal IN of the buffer. The transistor MP1, which has the function of a controlled electronic switch, has its gate electrode connected to the input terminal IN of the buffer. The second circuit branch of the driver stage 14 comprises a p-channel MOS transistor MP3 connected in the so-called diode arrangement, that is, with its gate and drain connected to one another, in series with a p-channel MOS transistor MP2 having the function of a controlled electronic switch. The common electrodes of the transistor MP3 are connected to the gate electrode of the output transistor MPOUT and the gate electrode of the transistor MP2 is connected to the output terminal OUT of the buffer.

[0013] The driver stage 15, as can be seen from Figure 3, is constituted by a third branch (MP4, MN1) and by a fourth branch (MN3, MN2) having structures duplicating those of the first and second branches of the driver stage 14.

[0014] Before the operation of the buffer of Figure 3 is 'examined, it is appropriate to make some remarks relating to the nature and the dimensions of the transistors which form parts thereof. The dimensions of the output transistors MPOUT and MNOUT are determined by the same criteria as are used for the buffer of the prior art, that is, on the basis of the maximum value of the supply voltage and on the maximum value of the current to be supplied to a resistive load during direct-current operation. The transistor MP2 must operate substantially is a switch and must therefore have as low as possible an impedance when it is made conductive. The transistor MP3 must conduct a current which is a predetermined fraction of the current of the output transistor MPOUT and will therefore have dimensions correspondingly correlated with those of the transistor MPOUT (typically, it will have the same channel length and a width which is a fraction of the width of MPOUT). The transistor MN4 is intended to operate in saturation conditions, that is, with a large impedance, and must be able to supply the necessary current to MP3. The transistor MP1 is intended to operate as a switch for rapidly interrupting conduction of the output transistor MPOUT when required and is therefore dimensioned accordingly. Wholly similar remarks may be made with regard to the dimensions of the transistors of the driver stage 15 of the output transistor MNOUT.

[0015] The operation of the buffer during a switch from 0 to 1 of a digital signal applied to the input terminal IN will now be considered with reference to Figure 4. It can easily be seen that, in the absence of a signal, with the input IN at level 0, that is, at the earth potential, the output OUT is also at 0, that is, MNOUT is conductive (on) and MPOUT is non-conductive (off). When the signal is applied to the input IN, immediately after the leading edge from 0 to 1, MP4 becomes non-conductive (off) and MN1 becomes conductive (ON). The output transistor MNOUT switches off because its gate electrode DN goes to 0. At the same time, in the driver stage 14, MP1 switches off and MN4 switches on. Since the output OUT is at 0, MP2 is on so that a current flows through MP2, MP3 and MN4, connected in series. At the gate electrode DP of the output transistor MPOUT, there will be a voltage VDD-VDS(MP2)-VTH(MP3)-VOD(MP3), that is, the supply voltage VDD, minus the voltage drop in MP2 in saturation conditions, minus the threshold voltage of MP3, minus the voltage beyond the threshold (overdrive) due to the current imposed by MN4 in MP3. By way of indication, the voltage at the node DP will be below the supply voltage VDD by a value of between 0.7 and 1.5V, according to the relative dimensions of the various transistors. In these conditions, the output transistor MPOUT, which was initially off, starts to conduct a current substantially proportional to that which passes through the transistor MP3 and to charge the capacitance of the load 13. The coefficient of proportionality is determined by the scale factor, that is, by the dimensional ratio between MPOUT and MP3. This situation is maintained throughout the time for which MP2 remains on. When the voltage at the output terminal OUT reaches a value equal to VDD minus the threshold of MP2, minus the overdrive of MP2 (very small if MP2 is of a suitable size), MP2 switches off, interrupting the flow of current through MP3 and MN4. Since MN4 is still on because the input IN is at high level (VDD), the node DP goes to 0, MPOUT is switched on and the output OUT goes to VDD. The rise in the voltage at the output OUT to VDD takes place with a constant rate of change (slew rate) for the greater portion of its swing, that is, the portion determined substantially solely by the current reflected by MP3 on MPOUT. The small residual swing is controlled by the zeroing rate of the node DP, that is, by the capacitance associated therewith (substantially the gate capacitance of MPOUT) and does not lead to a substantial increase in the current of the output transistor MPOUT which operates in the linear zone in these conditions.

[0016] When the input IN goes from 1 to 0, the output

OUT switches from 1 to 0 in a manner precisely mirroring that described above.

[0017] As is clear from the foregoing, in the buffer according to the invention, the current delivered to the load 13 or absorbed thereby during the transitions of the signal is substantially independent of the load and is determined basically by the dimensions of the components of the driver stages. It should also be noted that, in contrast with the known buffer shown in Figure 2, in which the slow voltage variation front at each of the gate electrodes of the output transistors is inactive until the threshold of the respective output transistor is exceeded, with a consequent delay of the output signal, the response of the buffer according to the invention is very rapid since the charging of the gate capacitances of the output transistors takes place by means of the series connection of a transistor connected as a diode (MP3 or MN3) and of a transistor with the function of a switch (MP2 or MN2), both of which have low resistance. Finally, the area required to produce the buffer according to the invention is very small, by virtue of the low number of components.

[0018] According to the embodiment shown in Figure 5, the transistors MN4 and MP4 of Figure 3, which have the function of current generators, are replaced by constant-current generators IGEN1 and IGEN2 in series with respective transistors MN5 and MP5 having the function of switches controlled by the input signal. The constant-current generators IGEN1 and IGEN2 may be formed with the use of n-channel and p-channel transistors, respectively, connected as current mirrors to a biasing circuit. A biasing circuit may be provided in the integrated circuit for other purposes so that, in this case, further comoonents are not necessary to complete the buffer, or the biasing circuit may be formed appropriately.

[0019] Figure 6 shows a possible embodiment of the biasing circuit. The transistors MIGEN1 and MIGEN2 which perform the functions of the generators IGEN1 and IGEN2 of Figure 5 are connected as current mirrors to two transistors, MN6 and MP6, respectively, which are connected as diodes in series with a resistor R, between the supply terminals VDD and earth. The current reflected is determined substantially solely by the supply voltage and by the resistance R and, to a large extent, is insensitive to variations of the process parameters and of the operating temperature of the circuit. It should also be noted that the transistors MIGEN1 and MIGEN2 are conductive only during the transitions in the level of the input signal, by virtue of the action of the series transistors MN4 and MP5, respectively, so that their contribution to the consumption of electrical energy is very limited.

[0020] The buffer may also be used to control an internal load of the integrated circuit which contains the buffer, rather than for controlling an external load as in the embodiments described.

Claims

1. An output buffer for digital signals having an output stage comprising a first output MOS transistor of a first type (P) and a second MOS transistor of a second type (N) with respective source electrodes connected to a first supply terminal (VDD) and to a second supply terminal (earth), respectively, drain electrodes connected together to an output terminal (OUT) of the buffer, and gate electrodes connected to an input terminal (IN) of the buffer by means of a first driver stage (14) and a second driver stage (15), respectively, **characterized in that**:

   the first driver stage (14) comprises:

   a first circuit branch comprising first current-generator means (MN4) connected between the gate electrode (DP) of the first output transistor (MPOUT) and the second supply terminal (earth) and a first controlled electronic switch (MP1) connected between the gate electrode (DP) of the first output transistor (MPOUT) and the first supply terminal (VDD) and having a control electrode connected to the input terminal (IN) of the buffer, and
   a second circuit branch comprising a first MOS transistor of the first type (P) connected as a diode (MP3) in series with a second controlled electronic switch (MP2) between the gate electrode (DP) of the first output transistor (MPOUT) and the first supply terminal (VDD), the second electronic switch (MP2) having a control terminal connected to the output terminal (OUT) of the buffer, and

   the second driver stage (15) comprises:

   a third circuit branch comprising second current-generator means (MP4) connected between the gate electrode (DN) of the second output transistor (MNOUT) and the first supply terminal (VDD) and a third controlled electronic switch (MN1) connected between the gate electrode (DN) of the second output transistor (MNOUT) and the second supply terminal (earth) and having a control electrode connected to the input terminal (IN) of the buffer, and
   a fourth circuit branch comprising a second MOS transistor of the second type (N) connected as a diode (MN3) in series with a fourth controlled electronic switch (MN2) between the gate electrode (DN) of the second output transistor (MNOUT) and the second supply terminal (earth), the fourth

electronic switch (MN2) having a control terminal connected to the output terminal (OUT) of the buffer.

2. An output buffer according to Claim 1 in which the first current-generator means comprises a third MOS transistor (MN4) of the second type (N) having its gate terminal connected to the input terminal (IN) of the buffer and the second current-generator means comprises a fourth MOS transistor (MP4) of the first type (P) having its gate terminal connected to the input terminal (IN) of the buffer.

3. An output buffer according to Claim 1 in which the first current-generator means comprises a first current generator (IGEN1) in series with a fifth controlled electronic switch (MN5) having a control terminal connected to the input terminal (IN) of the buffer and the second current-generator means comprises a second current generator (IGEN2) in series with a sixth controlled electronic switch (MP5) having a control terminal connected to the input terminal (IN) of the buffer.

Patentansprüche

1. Ein Ausgangspuffer für Digitalsignale mit einer Ausgangsstufe, der einen ersten Ausgangs-MOS-Transistor eines ersten Typs (P) und einen zweiten MOS-Transistor eines zweiten Typs (N) mit jeweiligen SourceElektroden, die mit einem ersten Versorgungsanschluß (VDD) bzw. mit einem zweiten Versorgungsanschluß (Erde) verbunden sind, Drain-Elektroden, die zusammen mit einem Ausgangsanschluß (OUT) des Puffers verbunden sind, und Gate-Elektroden aufweist, die mit einem Eingangsanschluß (IN) des Puffers mittels einer ersten Treiberstufe (14) bzw. einer zweiten Treiberstufe 15 verbunden sind, **dadurch gekennzeichnet, daß**

die erste Treiberstufe (14) folgende Merkmale aufweist:

eine erste Schaltungsverzweigung, die eine erste Stromerzeugungseinrichtung (MN4), die zwischen die Gate-Elektrode (DP) des ersten Ausgangstransistors (MPOUT) und den zweiten Versorgungsanschluß (Erde) geschaltet ist, und einen ersten gesteuerten elektronischen Schalter (MP1) aufweist, der zwischen die Gate-Elektrode (DP) des ersten Ausgangstransistors (MPOUT) und den ersten Versorgungsanschluß (VDD) geschaltet ist und eine Steuerelektrode aufweist, die mit dem Eingangsanschluß (IN) des Puffers verbunden ist, und

eine zweite Schaltungsverzweigung, die einen ersten MOS-Transistor des ersten Typs (P) aufweist, der als eine Diode (MP3) mit einem zweiten gesteuerten elektronischen Schalter (MP2) zwischen die Gate-Elektrode (DP) des ersten Ausgangstransistors (MPOUT) und den ersten Versorgungsanschluß (VDD) in Reihe geschaltet ist, wobei der zweite elektronische Schalter (MP2) einen Steueranschluß aufweist, der mit dem Ausgangsanschluß (OUT) des Puffers verbunden ist, und

die zweite Treiberstufe (15) folgende Merkmale aufweist:

eine dritte Schaltungsverzweigung, die eine zweite Stromerzeugungseinrichtung (MP4), die zwischen die Gate-Elektrode (DN) des zweiten Ausgangstransistors (MNOUT) und den ersten Versorgungsanschluß (VDD) geschaltet ist, und einen dritten gesteuerten elektronischen Schalter (MN1) aufweist, der zwischen die Gate-Elektrode (DN) des zweiten Ausgangstransistors (MNOUT) und den zweiten Versorgungsanschluß (Erde) geschaltet ist und eine Steuerelektrode aufweist, die mit dem Eingangsanschluß (IN) des Puffers verbunden ist, und

eine vierte Schaltungsverzweigung, die einen zweiten MOS-Transistor des zweiten Typs (N) aufweist, der als eine Diode mit einem vierten gesteuerten elektronischen Schalter (MN2) zwischen die Gate-Elektrode (DN) des zweiten Ausgangstransistors (MNOUT) und den zweiten Versorgungsanschluß (Erde) in Reihe geschaltet ist, wobei der vierte elektronische Schalter (MN2) einen Steueranschluß aufweist, der mit dem Ausgangsanschluß (OUT) des Puffers verbunden ist.

2. Ein Ausgangspuffer gemäß Anspruch 1, bei dem die erste Stromerzeugungseinrichtung einen dritten MOS-Transistor (MN4) des zweiten Typs (N) aufweist, der den Gate-Anschluß desselben mit dem Eingangsanschluß (IN) des Puffers verbunden aufweist, und die zweite Stromerzeugungseinrichtung einen vierten MOS-Transistor (MP4) des ersten Typs (P) aufweist, der den Gate-Anschluß desselben mit dem Eingangsanschluß (IN) des Puffers verbunden aufweist.

3. Ein Ausgangspuffer gemäß Anspruch 1, bei dem die erste Stromerzeugungseinrichtung einen ersten Stromgenerator (IGEN1) in Reihe mit einem fünften gesteuerten elektronischen Schalter (MN5) aufweist, der einen Steueranschluß aufweist, der mit dem Eingangsanschluß (IN) des Puffers verbunden ist, und die zweite Stromerzeugungseinrichtung einen zweiten Stromgenerator (IGEN2) in Reihe ist

einem sechsten gesteuerten elektronischen Schalter (MP5) aufweist, der einen Steueranschluß aufweist, der mit dem Eingangsanschluß (IN) des Puffers verbunden ist.

Revendications

1. Circuit tampon de sortie destiné à des signaux numériques comportant un étage de sortie comprenant un premier transistor MOS de sortie d'un premier type (P) et un second transistor MOS d'un second type (N), les électrodes de source respectives étant reliées à première borne d'alimentation (VDD) et à une seconde borne d'alimentation (la masse), respectivement, les électrodes de drain étant reliées ensemble sur une borne de sortie (OUT) du circuit tampon, et les électrodes de grille étant reliées à une borne d'entrée (IN) du circuit tampon au moyen d'un premier étage d'attaque (14) et d'un second étage d'attaque (15) respectivement, **caractérisé en ce que :**

   le premier étage d'attaque (14) comprend :

   une première branche de circuit constituée d'un premier moyen de générateur de courant (MN4) relié entre l'électrode de grille (DP) du premier transistor de sortie (MPOUT) et la seconde borne d'alimentation (la masse) et d'un premier commutateur électronique commandé (MP1) relié entre l'électrode de grille (DP) du premier transistor de sortie (MPOUT) et la première borne d'alimentation (VDD) et présentant une électrode de commande reliée à la borne d'entrée (IN) du circuit tampon, et une seconde branche de circuit constituée d'un premier transistor MOS du premier type (P) relié en qualité de diode (MP3) en série avec un second commutateur électronique commandé (MP2) entre l'électrode de grille (DP) du premier transistor de sortie (MPOUT) et la première borne d'alimentation (VDD), le second commutateur électronique (MP2) comportant une borne de commande reliée à la borne de sortie (OUT) du circuit tampon, et

   le second étage d'attaque (15) comprend :

   une troisième branche de circuit constituée d'un second moyen de générateur de courant (MP4) relié entre l'électrode de grille (DN) du second transistor de sortie (MNOUT) et la première borne d'alimentation (VDD) et d'un troisième commutateur électronique commandé (MN1) relié entre l'électrode de grille (DN) du second transistor de sortie (MNOUT) et la seconde borne d'alimentation (la masse) et présentant une électrode de commande reliée à la borne d'entrée (IN) du circuit tampon, et une quatrième branche de circuit constituée d'un second transistor MOS du second type (N) relié en qualité de diode (MN3) en série avec un quatrième commutateur électronique commandé (MN2) entre l'électrode de grille (DN) du second transistor de sortie (MNOUT) et la seconde borne d'alimentation (la masse), le quatrième commutateur électronique (MN2) comportant une borne de commande reliée à la borne de sortie (OUT) du circuit tampon.

2. Circuit tampon de sortie selon la revendication 1, dans lequel le premier moyen de générateur de courant comprend un troisième transistor MOS (MN4) du second type (N) ayant sa borne de grille reliée à la borne d'entrée (IN) du circuit tampon et le second moyen de générateur de courant comprend un quatrième transistor MOS (MP4) du premier type (P) ayant sa borne de grille reliée à la borne d'entrée (IN) du circuit tampon.

3. Circuit tampon de sortie selon la revendication 1, dans lequel le premier moyen de générateur de courant comprend un premier générateur de courant (IGEN1) en série avec un cinquième commutateur électronique commandé (MN5) comportant une borne de commande reliée à la borne d'entrée (IN) du circuit tampon et le second moyen de générateur de courant comprend un second générateur de courant (IGEN2) en série avec un sixième commutateur électronique commandé (MP5) comportant une borne de commande reliée à la borne d'entrée (IN) du circuit tampon.

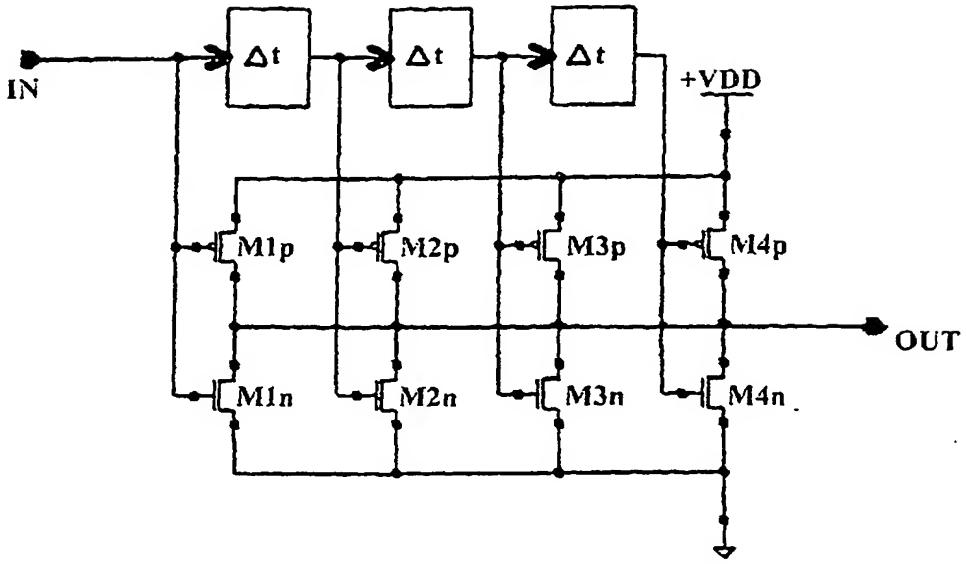
IN
Δt
Δt
Δt
+VDD
M1p
M2p
M3p
M4p
OUT
M1n
M2n
M3n
M4n

FIG. 1

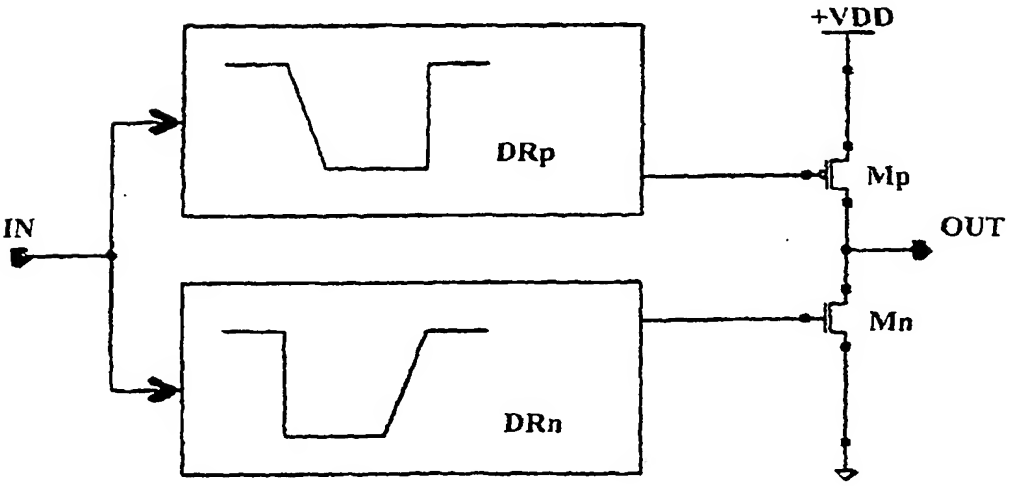
+VDD
DRp
Mp
IN
OUT
Mn
DRn

FIG. 2

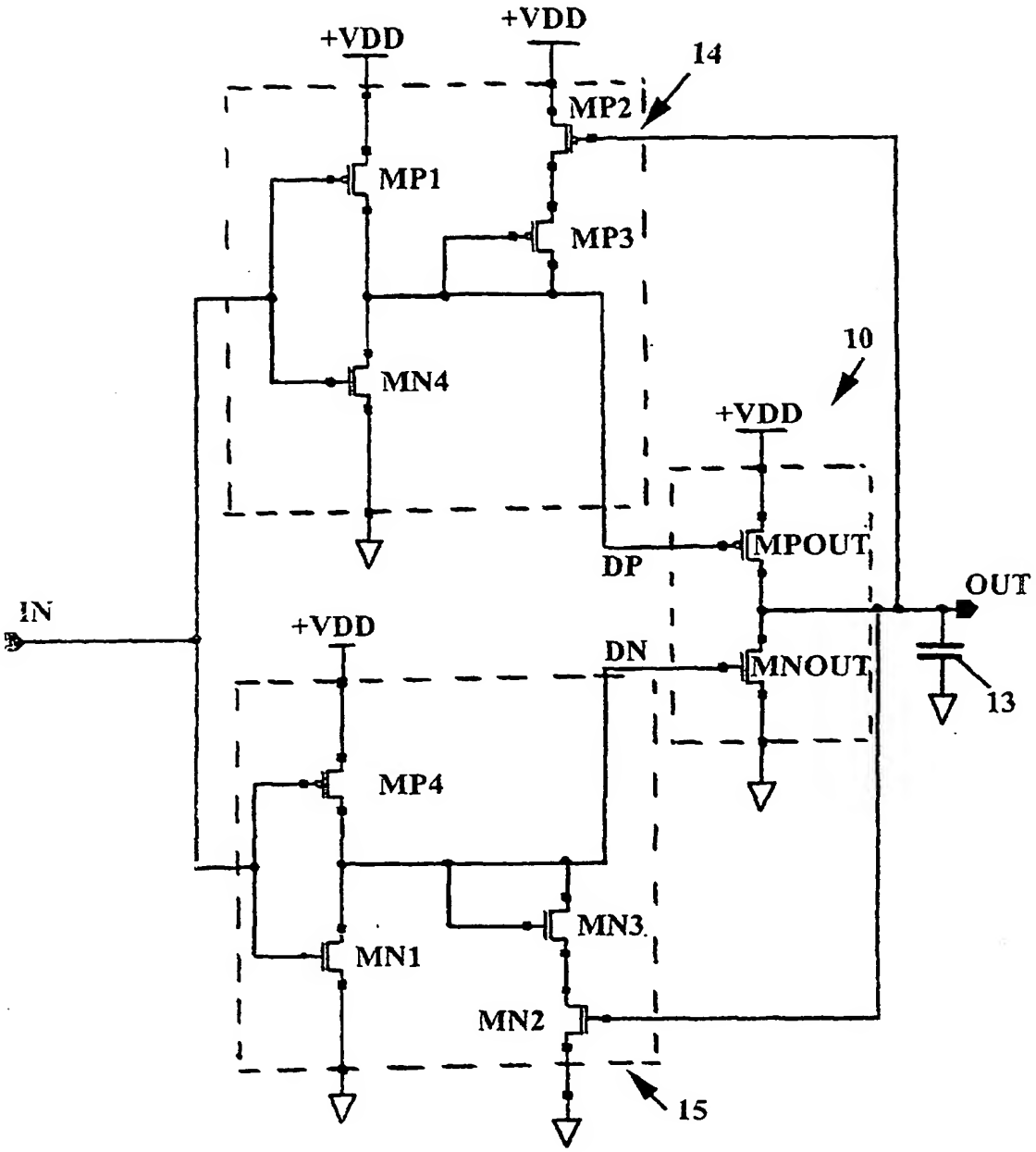
+VDD
+VDD
14
MP2
MP1
MP3
10
MN4
+VDD
MPOUT
DP
OUT
IN
+VDD
DN
MNOUT
13
MP4
MN3
MN1
MN2
15

FIG. 3

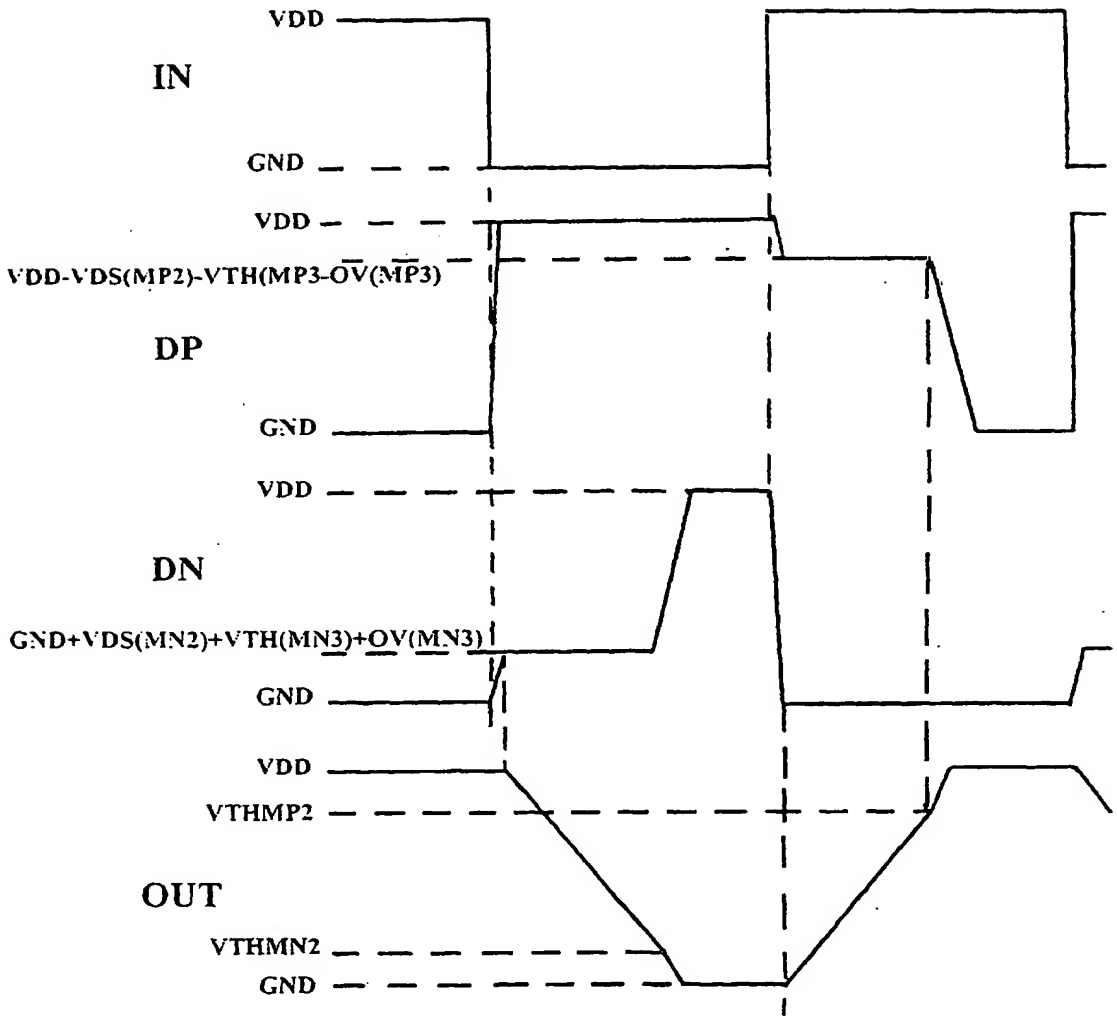
VDD
IN
GND
VDD
VDD-VDS(MP2)-VTH(MP3-OV(MP3)
DP
GND
VDD
DN
GND+VDS(MN2)+VTH(MN3)+OV(MN3)
GND
VDD
VTHMP2
OUT
VTHMN2
GND

FIG. 4

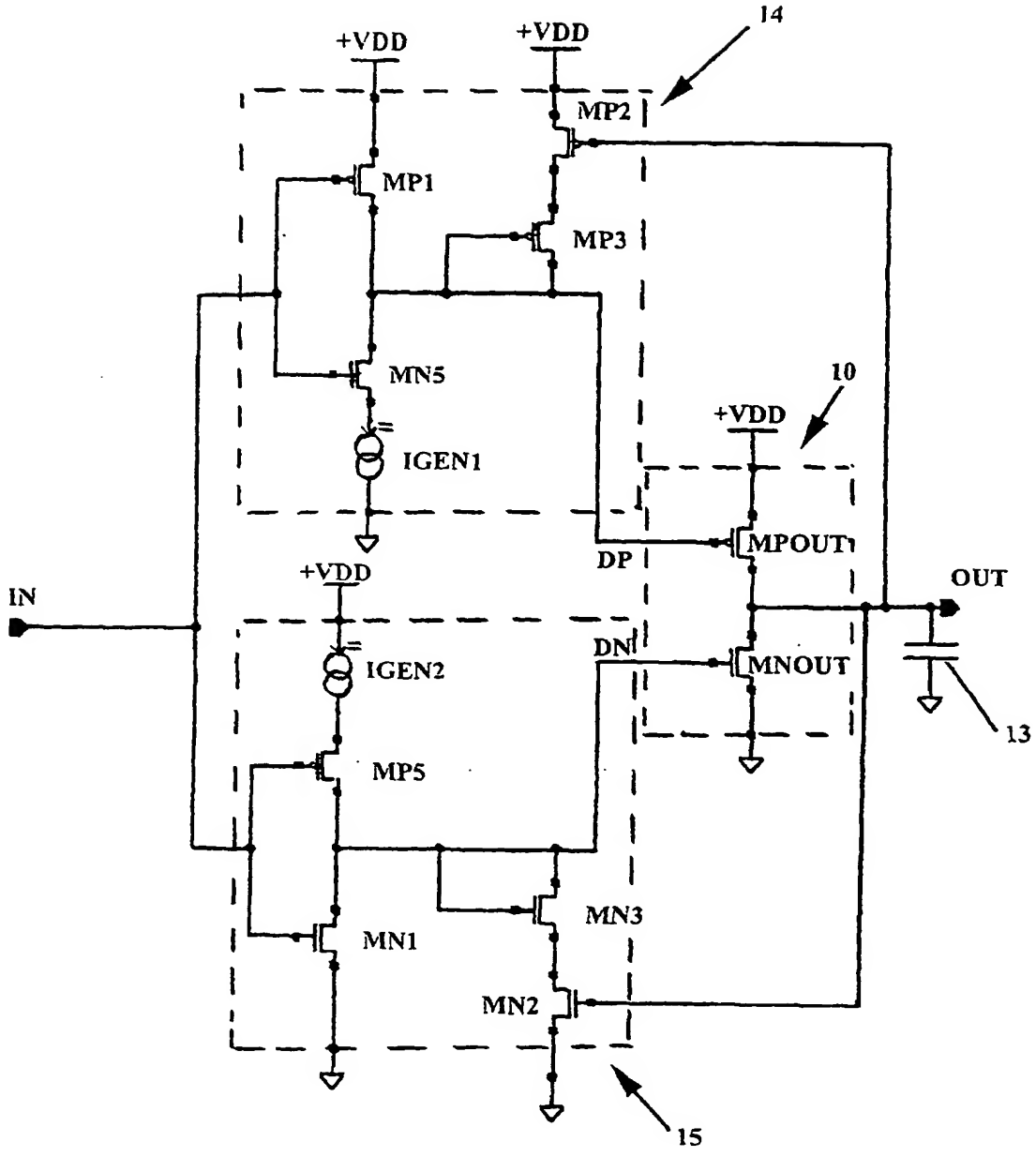
+VDD
+VDD
14
MP2
MP1
MP3
MN5
10
+VDD
IGEN1
MPOUT
DP
+VDD
OUT
IN
DN
MNOUT
IGEN2
13
MP5
MN3
MN1
MN2
15

FIG. 5

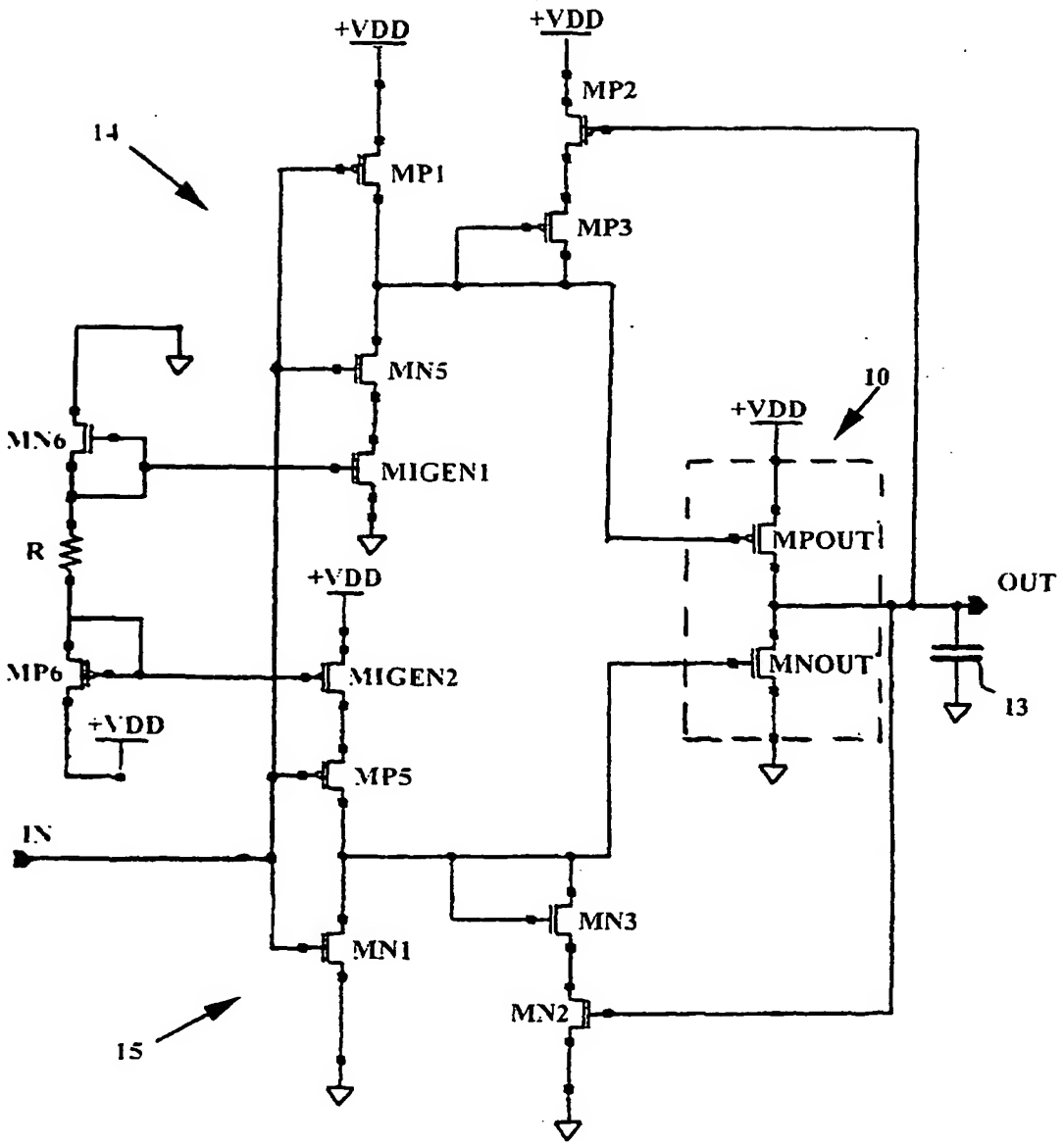
+VDD
+VDD
MP2
14
MP1
MP3
MN5
10
+VDD
MN6
MIGEN1
MPOUT
R
+VDD
OUT
MP6
MIGEN2
MNOUT
+VDD
13
MP5
IN
MN3
MN1
MN2
15

FIG. 6